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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/585,643	07/07/2006	**Takanori Okada**	056937-0295	5463

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EXAMINER	
GIARDINO JR, MARK A	

ART UNIT	PAPER NUMBER
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/585,643	OKADA ET AL.	
	Examiner	Art Unit	
	MARK A. GIARDINO JR	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/7/2006, 5/8/2007, 10/19/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/585,643 has a total of 18 claims pending in the application, there are 18 independent claims and 0 dependent claims, all of which are ready for examination by the examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. ' 1.63**.

STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

As required by **M.P.E.P. ' 201.14(c)**, acknowledgment is made of applicant's claim for priority based on an application filed in JP 2004-003787 with a filing date of January 9, 2004.

INFORMATION CONCERNING DRAWINGS

Drawings

Figures 7-11 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled “Replacement Sheet” in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

As required by **M.P.E.P. ' 609 (C)**, the applicant's submission of the Information Disclosure Statements, dated 7/07/2006, 5/08/2007, and 10/19/2007 are acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P. ' 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

REJECTIONS NOT BASED ON PRIOR ART

DEFICIENCIES IN THE SPECIFICATION

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. ' 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 4, 7, 9, 10, 13, 15, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by **Chiba (US 6,401,166).**

Regarding Claim 1, Chiba teaches a recording medium of non-volatile semiconductor (flash memory 1 of Figure 1) comprising a partition management information region (master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26) and a partition region (data regions of Figure 4), wherein an information on a start position of the partition region is recorded in the partition management information region (master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26), the start position information includes a value at which a predetermined region ("empty region" of Figure 4) is secured between a terminal end of the partition management information region and a starting end of the partition region (the partition information in the master boot region contains information on the "position of a beginning page of each partition" and the "position of an end page of each partition" and thus contains a value indicating where each partition [including the empty region] begins and ends, Column 8 Lines 27-32), and the region secured between the terminal end of the partition management information region and the starting end of the partition region is in a state where data is physically erased (see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block", and at the end of the process of Figure 10 the master boot region is created while the other regions

remain in a state where data is physically erased, see Format processing information on Column 12 Line 52 to Column 13 Line 25).

Regarding Claim 3, Chiba teaches a recording medium of non-volatile semiconductor (flash memory 1 of Figure 1) in which information is recorded according to a recording format of a predetermined file system (FAT file system format, which uses “a table indicating an allocation of the file”, Column 8 Line 64) wherein a region which is not used for the recording is included in the recording format of the file system (“empty region” of Figure 4, which is used “for coinciding a head and end of the block…with those of a cluster”, and is thus not used for the recording, Column 8 Lines 34-38), and the region which is not used for the recording is in a state where data is physically erased (see step s401 in Figure 10, where there is a command to “erase each block and then erase the storage content of each block”, and at the end of the process of Figure 10 the master boot region is created while the other regions remain in a state where data is physically erased, see Format processing information on Column 12 Line 52 to Column 13 Line 25).

Regarding Claim 4, Chriba teaches a recording medium of non-volatile semiconductor (flash memory 1 of Figure 1) in which information is recorded according to a recording format of FAT file system (Chriba uses the FAT file system format, which uses “a table indicating an allocation of the file”, Column 8 Line 64), wherein a partition boot information region (master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26) and a file allocation table region are included (File Allocation Table of

Figure 4), an information on number of reserved sectors (in the “empty region” of Figure 4) is recorded in the partition boot information region (the partition boot information records the “total pages included in each partition”, Column 8 Line 33, where the pages are equivalent to sectors), the information on the number of the reserved sectors includes a value at which a predetermined region (the “empty region” of Figure 4) is secured between a terminal end of the partition boot information region and a starting end of the file allocation table region (the partition information in the master boot region contains information on the "position of a beginning page of each partition" and the "position of an end page of each partition" and thus contains a value indicating where each partition begins and ends, Column 8 Lines 30-32, and the empty region is shown between the boot information region and file allocation table region in Figure 4), and the region secured between the terminal end of the partition boot information region and the starting end of the file allocation table region is in a state where data is physically erased (see step s401 in Figure 10, where there is a command to “erase each block and then erase the storage content of each block”, and at the end of the process of Figure 10 the master boot region is created while the other regions remain in a state where data is physically erased, see Format processing information on Column 12 Line 52 to Column 13 Line 25).

Claim 7 is the method equivalent to Claim 1, and is rejected under similar rationale.

Claim 9 is the method equivalent to Claim 3, and is rejected under similar rationale.

Claim 10 is the method equivalent to Claim 4, and is rejected under similar rationale.

Claim 13 is the information recording format equivalent to Claim 1, and is rejected under similar rationale.

Claim 15 is the information recording format equivalent to Claim 3, and is rejected under similar rationale.

Claim 16 is the information recording format equivalent to Claim 4, and is rejected under similar rationale.

Claim Rejections - 35 USC ' 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 8, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiba in view of Mine (US 6,182,240).

Regarding Claim 2, Chiba teaches a recording medium of non-volatile semiconductor (flash memory 1 of Figure 1) comprising a partition management information region (master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26) and a partition region (data regions of Figure 4) and N pieces (N is an integer at

least two) of partition regions (note the multiple N data regions of Figure 4), wherein an information on start positions of the N pieces of partition regions is recorded in the partition management information region (master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26).

However, Chiba does not teach additional partitions between the Nth and (N-1)th partition regions. Mine teaches additional replacement areas between the data areas (Figure 2 in Mine). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented such replacement areas in the device of Chiba. Since the data areas are between all data regions (shown in Figure 2 in Mine), there would be one between the terminal end of the (N-1)th partition region and a starting end of the Nth partition region, and after a format, the data on all the data area blocks is physically erased (see step s401 in Figure 10, where there is a command to “erase each block and then erase the storage content of each block”, and at the end of the process of Figure 10 the master boot region is created while the other regions remain in a state where data is physically erased, see Format processing information on Column 12 Line 52 to Column 13 Line 25).

As motivation, the replacement areas allow one to replace defective portions of the memory (Column 6 Lines 45-48 in Mine). Thus, by combining the devices, additional benefits are obtained.

Claim 8 is the method equivalent of Claim 2, and is rejected under similar

rationale.

Claim 15 is the information recording format equivalent to Claim 2, and is rejected under similar rationale.

Claims 5, 11, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiba in view of Nakamura et al (US 6,873,789).

Regarding Claim 5, Chiba teaches a recording medium of non-volatile semiconductor (flash memory 1 of Figure 1) in which information is recorded according to a file system, wherein a partition descriptor information region (master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26) and a file system specific region are included (Chriba uses the FAT file system format, which uses “a table indicating an allocation of the file”, Column 8 Line 64), an information on a start position of the space bit map region is recorded in the partition descriptor information region (the partition information in the master boot region contains information on the "position of a beginning page of each partition", Column 8 Lines 30-32), the start position information includes a value at which a predetermined region (“empty region” of Figure 4) is secured prior to a starting end of the file system specific region, and the region secured prior to the starting end of the space bit map region (the empty region is shown between the boot information region and file allocation table region in Figure 4) is in a state where data is physically erased (see step s401 in Figure 10, where there is a command to “erase each block and then erase the storage content of each block”, and at the end

of the process of Figure 10 the master boot region is created while the other regions remain in a state where data is physically erased, see Format processing information on Column 12 Line 52 to Column 13 Line 25).

However, Chriba does not teach using the UDF file system with a space bit map region. Nakamura teaches a UDF file system (Column 6 Lines 22-25) with a space bit map in memory (Column 12 Lines 52-53). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used the space bit map for the file system specific region of Chriba and to use a UDF file system in place of the FAT file system, so that the memory device of Chriba can be compatible with operating systems that use the UDF file system.

Claim 11 is the method equivalent to Claim 5, and is rejected under similar rationale.

Claim 17 is the information recording format equivalent to Claim 5, and is rejected under similar rationale.

Claims 6, 12, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiba in view of Mine (US 6,182,240).

Regarding Claim 6, Chiba teaches a recording medium of non-volatile semiconductor (flash memory 1 of Figure 1) in which information is recorded according to a recording format of FAT file system (Chriba uses the FAT file system format, which uses “a table indicating an allocation of the file”, Column 8 Line 64), wherein a user data

region comprising a plurality of clusters (data regions of Figure 4, which also shows a plurality of clusters among the data regions) and a file allocation table region (FAT region of Figure 4) are included, an information on a state of each cluster in the user data region is recorded in the file allocation table region (since the CPU can tell if a cluster is empty by analyzing the content of the FAT, the FAT records information on the state of the clusters, Column 14 Lines 3-4), the state information includes a value indicating if a particular cluster is a reserved cluster or an already-used cluster (the FAT can tell if a cluster is already used [or reserved] based on whether or not the cluster is empty, Column 14 Lines 3-4, also see step S504 of Figure 11), and a region of the cluster of the user data region corresponding to the particular cluster of the state information is in a state where data is physically erased (see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block", and at the end of the process of Figure 10 the master boot region is created while the other regions remain in a state where data is physically erased, see Format processing information on Column 12 Line 52 to Column 13 Line 25).

However, Chriba does not explicitly teach the FAT storing whether or not a sector is defective. Fukushima teaches a FAT that stores whether or not sectors are defective (Column 1 Lines 36-39). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have recorded defective sectors (and thus the clusters to which these sectors belong) in the device of Chriba to prevent one from using defective clusters, which may result in corrupted or unreadable data.

Claim 12 is the method equivalent to Claim 6, and is rejected under similar rationale.

Claim 18 is the information recording format equivalent to Claim 6, and is rejected under similar rationale.

CLOSING COMMENTS

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-18 have received a first action on the merits and are subject of a first action non-final.

DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Anthony Giardino whose telephone number is (571) 270-3565 and can normally be reached on Monday - Thursday 7:30am – 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M.A. Giardino

/M.G./

Patent Examiner
Art Unit 2185

June 9, 2008

/Sanjiv Shah/

Supervisory Patent Examiner, Art Unit 2185